What is claimed is:

1. A circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor; and

a keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.

2. The circuit of Claim 1, wherein

the second transistor is configured to receive a first cascode bias voltage at the gate of the second transistor, and wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

3. The circuit of Claim 1, wherein

the keeper switch circuit is configured to influence a resistance between the source and the gate of the second transistor in response to a control signal.

4. The circuit of Claim 1, wherein

the keeper switch circuit is configured to:

receive a control signal at the drain of the second transistor; and

couple the source of the second transistor to the gate of the second transistor if the control signal corresponds to a first logic level.

5. The circuit of Claim 4, wherein

the keeper switch circuit is further configured to isolate the source of the second transistor from the gate of the second transistor if the control signal corresponds to a second logic level.

6. The circuit of Claim 1, wherein

the keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the drain of the second transistor;

a source that is coupled to one of the source of the second transistor and the gate of the second transistor; and

a drain that is coupled to the other of the source of the second transistor and the gate of the second transistor.

7. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the one of the n-type transistor and the p-type transistor.

8. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and the p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

9. The circuit of Claim 1, further comprising:

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor; and

another keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the fourth transistor.

10. The circuit of Claim 9, wherein

the other keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the drain of the fourth transistor,

a source that is coupled to one of the source of the fourth transistor and the gate of the second transistor, and

a drain that is coupled to the other of the source of the fourth transistor and the gate of the second transistor.

11. A logic circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor, wherein the second transistor includes:

a gate that is coupled to a bias node,

a drain that is coupled to a first output node, and

a source that is coupled to a second output node;

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor, wherein the fourth transistor includes:

a gate that is coupled to the bias node,

a drain that is coupled to a first complement output node, and

a source that is coupled to a second complement output node,

a first keeper switch circuit that is coupled to the bias node, the second complement output node, and the second output node, and

a second keeper switch circuit that is coupled to the bias node, second output node, and the second complement output node.

12. The logic circuit of Claim 11, wherein

the second transistor is configured to receive a first cascode bias voltage at the bias node, wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

13. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to influence a resistance between the second output node and the bias node in response to a control signal.

14. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to:

receive a control signal at the second complement output node;

couple the second output node to the bias node if the control signal corresponds to a first logic level; and

isolate the second output node from the bias node if the control signal corresponds to a second logic level.

15. The logic circuit of Claim 11, wherein

the logic circuit is arranged to operate as a level shifter circuit.

16. The logic circuit of Claim 11, wherein

the first keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the second complement output node,

a source that is coupled to one of the second output node and the bias node, and

a drain that is coupled to the other of the second output node and the bias node.

17. The logic circuit of Claim 16, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

18. The logic circuit of Claim 11, wherein

the second keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the second output node,

a source that is coupled to one of the second complement output node and the bias node, and

a drain that is coupled to the other of the second complement output node and the bias node.

19. The logic circuit as in Claim 18, wherein

the first keeper switch circuit comprises a keeper transistor, and

wherein the second transistor is one of an n-type transistor and a p-type transistor, the keeper transistor is the other of the n-type transistor and the p-type transistor, and the fifth transistor is the other of the n-type transistor and the p-type transistor.

20. A circuit comprising:

a transistor that is configured as a cascode transistor; and

means for coupling a source of the transistor to a gate of the transistor if a voltage associated with a drain of the transistor corresponds to a first logic level.